WHAT IS CLAIMED IS

1. An optical sensor for producing an electrical signal in response to electromagnetic radiation, comprising :

a photodetector having an output supplying an electrical signal proportional to the intensity of the electromagnetic radiation striking the photodetector; and

an integrating circuit coupled with the output of the photodetector to accumulate the electrical signal from the photodetector, said integrating circuit comprising :

an operational amplifier having a non-inverting input connected to a non-zero bias voltage, an inverting input coupled to said photodetector, and at least one output;

an integrating voltage storage device having a first terminal coupled to the operational amplifier output and a second terminal coupled to the operational amplifier inverting input; and

switching circuitry for controlling timing of the integrating circuit and switching the integrating circuit between a reset phase and an integration phase,

wherein said switching circuitry includes means for balancing said operational amplifier and developing a voltage across said integrating voltage storage device during said reset phase, which voltage is substantially equal to said bias voltage, said first terminal of the integrating voltage storage device being pulled to a reference potential during said reset phase.

2. The optical sensor according to claim 1, wherein said integrating circuit further includes an output stage comprising a gate terminal connected to the operational amplifier output and an output terminal connected to said first terminal of the integrating voltage storage device,

said switching circuitry including :

a first switching device for connecting said operational amplifier output to said operational amplifier inverting input during said reset phase and for disconnecting said operational amplifier output from said operational amplifier inverting input during said integration phase; and

a second switching device for pulling said output stage output terminal to said reference potential during said reset phase and for releasing said output stage output terminal from said reference potential during said integration phase.

3. The optical sensor according to claim 2, wherein said output stage is a source-follower output stage.

4. The optical sensor according to claim 1, wherein said integrating voltage storage device is a MOS transistor operating in accumulation mode.

5. The optical sensor according to claim 1, wherein said photodetector is a reverse-biased photodiode.

6. The optical sensor according to claim 1, wherein said operational amplifier is a differential amplifier comprising a differential pair of transistors and having a half-folded cascode stage.

7. The optical sensor according to claim 2, wherein said integrating circuit further comprises a frequency compensation capacitor connected between said output stage gate terminal and said reference potential.

8. The optical sensor according to claim 7, wherein said frequency compensation capacitor is a MOS transistor with common source and drain terminals.

9. The optical sensor according to claim 2, wherein said first and second switching devices are CMOS transistors.

10. The optical sensor according to claim 2, wherein said first and second switching devices are both controlled by a single control signal.

11. The optical sensor according to claim 2, wherein said operational amplifier is a differential amplifier comprising a differential pair of transistors and having a half-folded cascode stage,

said integrating circuit further comprising a first current source coupled to said differential pair of transistors, a second current source coupled to said half-folded cascode stage and a third current source coupled to said output stage.

12. The optical sensor according to claim 11, wherein said second switching device is connected between said output stage output terminal and said third current source, said integrating circuit further comprising a fourth current source connected directly to said output stage output terminal.

13. The optical sensor according to claim 1 for use in an optical sensor array, further comprising first and second source-follower output stages for providing minimum and maximum electrical output signals allowing determination of the optical sensor within the array with the least, respectively the greatest, intensity.

14. The optical sensor according to claim 13, wherein said first source-follower output stage has a gate terminal connected to said first terminal of the integrating voltage storage device and a drain terminal connected to a first supply potential, a source terminal of said first source-follower output stage being coupled to a first external current source common to each optical sensor within the array,

and wherein said second source-follower output stage has a gate terminal connected to said operational amplifier output and a drain terminal connected to a second supply potential, a source terminal of said second source-follower output stage

being coupled to a second external current source common to each optical sensor within the array.

15. The optical sensor according to claim 1, wherein said non-zero bias voltage is supplied by voltage generating circuitry formed within said integrating circuit.

16. An integrating circuit for use with a photodetector having an output supplying an electrical signal proportional to the intensity of the electromagnetic radiation striking the photodetector, said integrating circuit comprising :

an operational amplifier having a non-inverting input connected to a non-zero bias voltage, an inverting input capable of being coupled to said photodetector, and at least one output;

an integrating voltage storage device having a first terminal coupled to the operational amplifier output and a second terminal coupled to the operational amplifier inverting input;

an output stage comprising a gate terminal connected to the operational amplifier output and an output terminal connected to said first terminal of the integrating voltage storage device; and

switching circuitry for controlling timing of the integrating circuit and switching the integrating circuit between a reset phase and an integration phase,

wherein said switching circuitry includes means for balancing said operational amplifier and developing a voltage across said integrating voltage storage device during said reset phase, which voltage is substantially equal to said bias voltage, said first terminal of the integrating voltage storage device being pulled to a reference potential during said reset phase.

17. The integrating circuit according to claim 16, wherein said switching circuitry includes :

a first means for connecting said operational amplifier output to said operational amplifier inverting input during said reset phase and for disconnecting said operational amplifier output from said operational amplifier inverting input during said integration phase; and

a second means for pulling said output stage output terminal to said reference potential during said reset phase and for releasing said output stage output terminal from said reference potential during said integration phase.

18. The integrating circuit according to claim 16, wherein said output stage is a source-follower output stage.

19. The integrating circuit according to claim 16, wherein said integrating voltage storage device is a MOS transistor operating in accumulation mode.

20. The integrating circuit according to claim 16, wherein said operational amplifier is a differential amplifier comprising a differential pair of transistors and having a half-folded cascode stage.